| Notice of Allowability | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/714,271 | YOU ET AL. | |
| | Examiner | Art Unit | |
| | Ron E. Pompey | 2812 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--*

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *8-7-06*.

2. ☒ The allowed claim(s) is/are *1-17*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS ( as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review ( PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   **Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).**

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

1. ☐ Notice of References Cited (PTO-892)
2. ☒ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 8-7-06
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

MICHAEL LEBENTRITT
SUPERVISORY PATENT EX.

## DETAILED ACTION

### *Allowable Subject Matter*

1. Claims 1-17 are allowed.

2. The following is an examiner's statement of reasons for allowance: the prior art of record, either singly or in combination, fails to disclose the limitations of:

forming a gate oxide for a gate of the LDMOS transistor between a source region and a drain region of the LDMOS transistor;

covering the gate oxide with a conductive material;

implanting, into a source region of the LDMOS transistor, a third impurity region with a second volume and a second surface area in the first surface area of the first impurity region, the third impurity region being of an opposite second type relative to the first type, the third impurity region being self aligned with respect to the gate of the LDMOS transistor;

forming a gate oxide (118,134) for a gate of the CMOS transistor between a source region and a drain region of the CMOS transistor, the gate oxide of the CMOS transistor being formed after implantation of the third impurity region, in combination with the other limitations of independent claim 1.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

## EXAMINER'S AMENDMENT

3. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with David Goren on June 8, 2006.

The application has been amended as follows:

Claims to be amended:

1. A method of fabricating an LDMOS transistor and a ~~conventional~~ CMOS transistor together on a substrate, the method comprising:

implanting, into a surface of a substrate, a first impurity region ~~(1304)~~ with a first volume and a first surface area, the first impurity region being of a first type;

implanting, into the surface of the substrate, a second impurity region ~~(106,122)~~; forming a gate oxide ~~(1306)~~ for a gate of the LDMOS transistor between a source region and a drain region of the LDMOS transistor;

covering the gate oxide with a conductive material ~~(1310)~~;

implanting, into a source region of the LDMOS transistor, a third impurity region ~~(1312)~~ with a second volume and a second surface area in the first surface area of the first impurity region, the third impurity region being of an opposite second type relative to the first type, the third impurity region being self aligned with respect to the gate of the LDMOS transistor;

forming a gate oxide ~~(118,134)~~ for a gate of the ~~conventional~~ CMOS transistor between a source region and a drain region of the ~~conventional~~ CMOS transistor, the gate oxide of the ~~conventional~~ CMOS transistor being formed after implantation of the third impurity region;

covering the gate oxide of the ~~conventional~~ CMOS transistor with a conductive material ~~(120,136)~~;

implanting, into the source region of the LDMOS transistor, a fourth impurity region ~~(1318)~~ with a third volume and a third surface area and a fifth impurity region ~~(1316)~~ with a fourth volume and a fourth surface area in the second surface area of the second impurity region, the fourth impurity region being of the first type, the fifth impurity region being of the opposite second type;

implanting, into the drain region of the LDMOS transistor, a sixth impurity region ~~(1320)~~ with a fifth volume and a fifth surface area, the sixth impurity region being of the first type;

implanting, into a source region of the ~~conventional~~ CMOS transistor, a seventh impurity region ~~(112,128)~~, the seventh impurity region being in the second impurity region; and

implanting, into a drain region of the ~~conventional~~ CMOS transistor, an eighth impurity region ~~(114,130)~~, the eighth impurity region being in the second impurity region.

5. The method of claim 1, further comprising implanting, into the drain region of the LDMOS transistor, a ninth impurity region ~~(1314)~~ with an eighth volume and an eighth

surface area in the first surface area of the first impurity region, the ninth impurity region being implanted with a spacing from the third impurity region, the ninth impurity region being of the first type.

10. The method of claim 5, wherein the implantation of the ninth impurity region is defined by a slit mask, the ninth impurity region forming multiple implants ~~(1812)~~ spaced apart relative to each other along a surface in the drain region of the LDMOS transistor.

11. The method of claim 1, wherein implanting the third impurity region includes implanting the third impurity region using a first implant ~~(802)~~ and a second implant ~~(804)~~.

14. The method of claim 1 , further comprising implanting, into the source region of the LDMOS transistor, a tenth impurity region ~~(1704)~~ with a ninth volume having a ninth surface area, and implanting, into the drain region of the LDMOS transistor, an eleventh impurity region ~~(1706)~~ with a tenth volume having a tenth surface area, the tenth impurity region and the eleventh impurity region being of the first type.

15. The method of claim 1, further comprising:

forming a field oxide ~~(2702)~~ on the drain region of the LDMOS transistor.

16. The method of claim 1 , wherein the ~~conventional~~ CMOS transistor is a ~~conventional~~ PMOS transistor and wherein:

the second impurity region ~~(106)~~ is of the first type; and

the seventh and eighth impurity regions are of the opposite second type.

17. The method of claim 1, wherein the ~~conventional~~ CMOS transistor is a ~~conventional~~ NMOS transistor and wherein'. the second impurity region ~~(122)~~ is of the opposite second type; and the seventh and eighth impurity regions are of the first type.

Cancel claims 18-26.

***Election/Restrictions***

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-17: Combination: LDMOS, LDMOS drain doping particulars and CMOS particulars.

II. Claims 18-26: Subcombination: LDMOS source doping particulars.

The inventions are distinct, each from the other because of the following reasons:

2. Inventions I and II are related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)). In the instant case, the combination as claimed does not require the

particulars of the subcombination as claimed because the subcombination requires a P-body implant not required by the combination. The subcombination has separate utility such as in a device, which does require the particulars of the combination (e.g. the LDMOS drain and CMOS particulars).

3. Because these inventions are independent or distinct for the reasons given above and the inventions require a different field of search (see MPEP § 808.02), restriction for examination purposes as indicated is proper.

4. This application contains claims directed to the following patentably distinct species:

Species I: gate for CMOS is not formed distinct from the gate of the LDMOS (Claims 18-22).

Species II: gate for CMOS is formed distinct from the gate of the LDMOS (Claims 18-22).

The species are independent or distinct because the formation of the gates (LDMOS and CMOS) requires different processes.

Applicant is required under 35 U.S.C. 121 to elect a single disclosed species for prosecution on the merits to which the claims shall be restricted if no generic claim is finally held to be allowable. Currently, no claims are generic.

Applicant is advised that a reply to this requirement must include an identification of the species that is elected consonant with this requirement, and a listing of all claims readable thereon, including any claims subsequently added. An argument that a claim

is allowable or that all claims are generic is considered nonresponsive unless accompanied by an election.

Upon the allowance of a generic claim, applicant will be entitled to consideration of claims to additional species which depend from or otherwise require all the limitations of an allowable generic claim as provided by 37 CFR 1.141. If claims are added after the election, applicant must indicate which are readable upon the elected species. MPEP § 809.02(a).

5. During a telephone conversation with David Goren on June 8, 2006 a provisional election was made without traverse to prosecute the invention of I, claims 1-17. Affirmation of this election must be made by applicant in replying to this Office action. Claims 18-26 withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

6. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ron E. Pompey whose telephone number is (571) 272-1680. The examiner can normally be reached on 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on (571) 272-1873. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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August 30, 2006

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